

Fig. 2

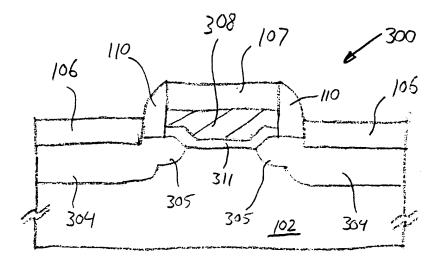
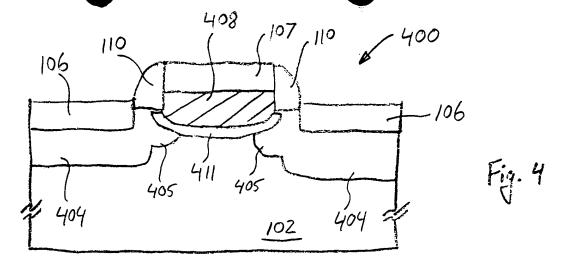


Fig.3

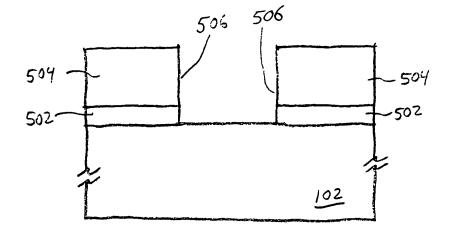
P6872

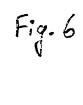




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70PS **3** 35500 7





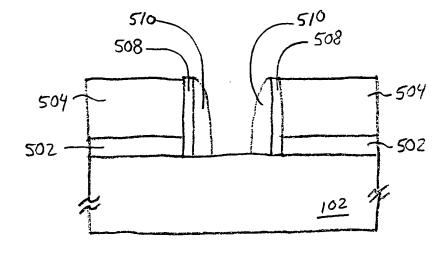


Fig. 7

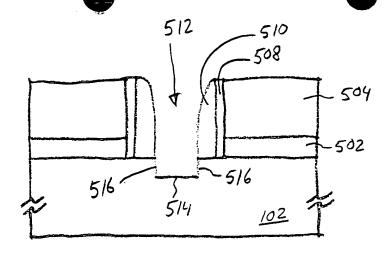


Fig. 8

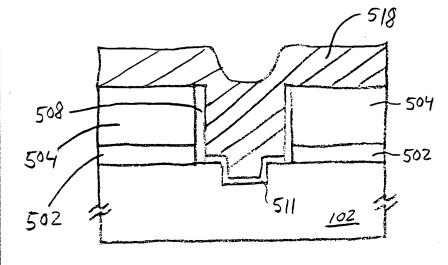


Fig. 9

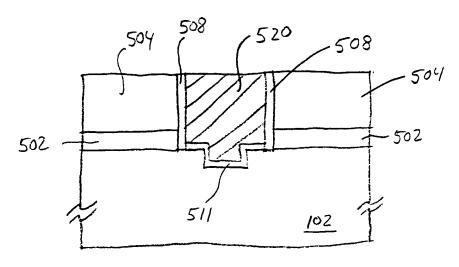


Fig. 10

P6892

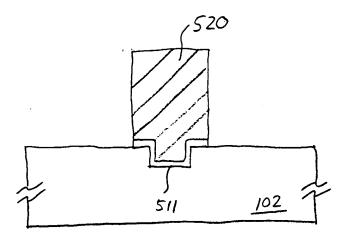


Fig. 11

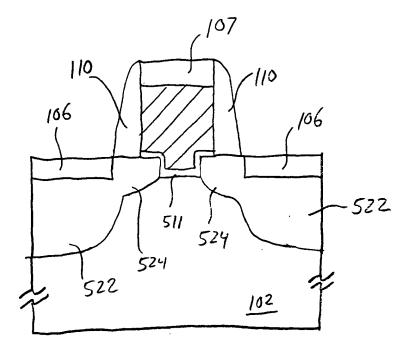
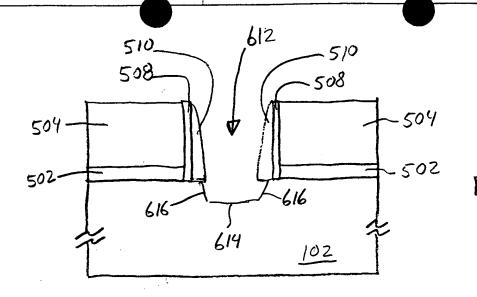


Fig. 12

P6892



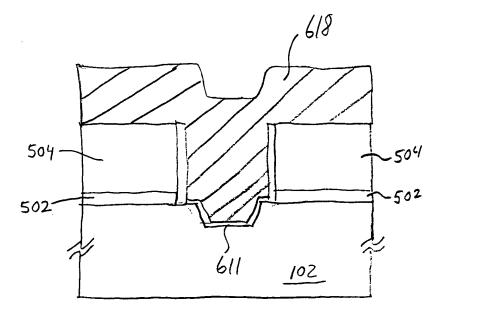


Fig. 14

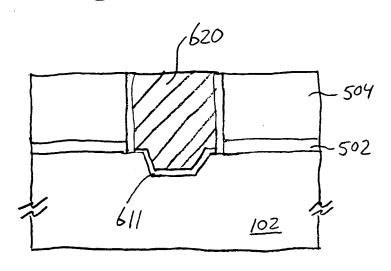


Fig. 15

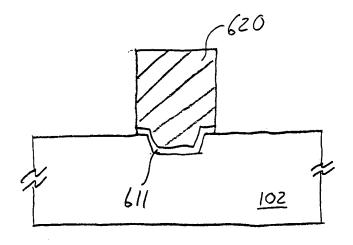


Fig. 16

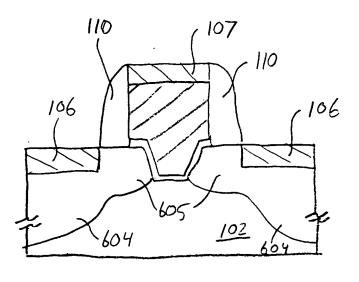


Fig. 17

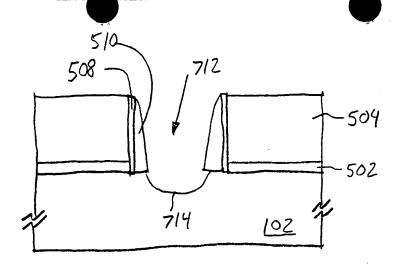


Fig. 18

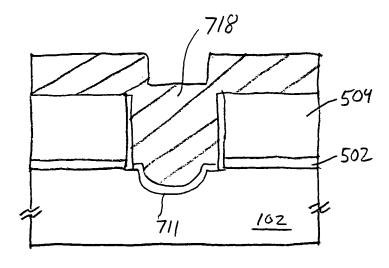


Fig. 19

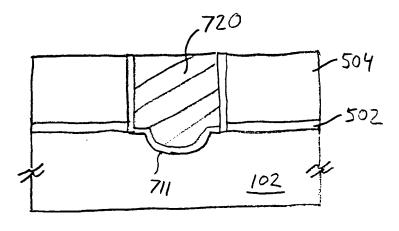


Fig. 20



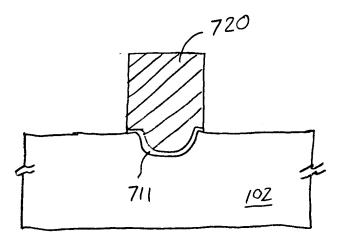


Fig. 21

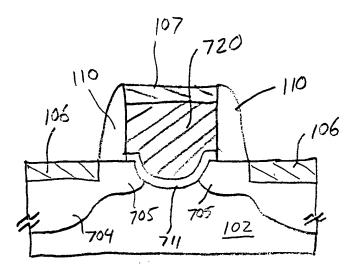


Fig. 22



	2302
Pattern openings in a damascene layer on a wafer	
	2304
Form spacers along the sidewalls of the openings in the damascene lay	/er
	2306
Form recesses in the wafer at locations defined by the openings	
	2308
Form gate dielectric layer over at least the recesses	
	2310
Form gate electrode over the gate dielectric	
	2312
Form source/drain extension aligned with gate electrode	